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December 14, 1999

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Assistant Commissioner for Patents
Washington, DC 20231

Presented for filing is a new original patent application of:

Applicant: KEITH DOW

Title: IMPROVED SIGNAL ROUTING BETWEEN A MEMORY CONTROL UNIT AND A MEMORY DEVICE

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Enclosed are the following papers, including those required to receive a filing date under 37 CFR 1.53(b):

	Pages
Specification	5
Claims	7
Abstract	1
Declaration	2
Drawing(s)	3

Enclosures:

— Assignment cover sheet and an assignment, 2 pages, and a separate $40 fee.
— Postcard.

Basic filing fee	$760
Total claims in excess of 20 times $18	$0
Independent claims in excess of 3 times $78	$78
Fee for multiple dependent claims	$0
Total filing fee:	$838

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Deborah L. Dean
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A check for the filing fee is enclosed. Please apply any other required fees or any credits to deposit account 06-1050, referencing the attorney docket number shown above.

If this application is found to be incomplete, or if a telephone conference would otherwise be helpful, please call the undersigned at (858) 678-5070.

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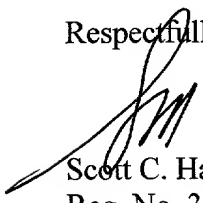
Respectfully submitted,



Scott C. Harris
Reg. No. 32,030
Enclosures
SCH/rpi
10010662.doc

Attorney's Docket No.: 10559/108001/P7643

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: IMPROVED SIGNAL ROUTING BETWEEN A MEMORY CONTROL UNIT AND A MEMORY DEVICE

APPLICANT: KEITH DOW

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IMPROVED SIGNAL ROUTING BETWEEN A MEMORY CONTROL UNIT AND A MEMORY DEVICE

Technical Field

The invention relates to signal routing between a memory control unit and a memory extender, such as a memory repeater hub device.

Background

FIG. 1 shows a typical computer system 100. The computer 100 includes a central processing unit (CPU) 105, or processor, and a memory repeater hub 110. A memory control unit (MCU) 120 controls the flow of data into and out of the memory unit 110. The memory unit 110 always includes volatile memory, such as dynamic random access memory (DRAM). The computer also includes other system components, including a non-volatile storage device, such as a hard disk 125, and a modem 130 to connect the computer 100 to a network 135.

The speed at which the computer operates depends in large part on the speed at which data is transferred between the processor 105 and the memory unit 110. One memory architecture in particular, known as the Rambus architecture, is designed to

transfer data to the processor 105 at very high rates, *e.g.*, 1.6 GB/s for a typical Rambus DRAM (RDRAM) module.

FIG. 2 shows a common routing configuration for signal lines connecting the MCU 120 to the memory unit. Each signal line 150 leaves the MCU 120 with a width of approximately 18 mils. Before reaching the appropriate pin 155 on the memory unit, the signal line 150 narrows, or "necks down", to a width of approximately 5 mils. The signal line 160 exiting the pin 155 also has a width of approximately 5 mils before expanding to a width of approximately 18 mils. A ground trace 165 separates the 5 mil neck down portions of the signal lines 150, 160. As a result of this congestion, the signal line 150 into the memory unit and the signal line 160 out of the memory unit often must be formed on different layers of the circuit board on which the MCU and memory unit reside.

Summary

A computer system includes a processor and a multi-layer circuit board having a memory unit, a memory control unit, and a data bus coupling the memory control unit to the memory unit. A first signal line is formed on a selected layer of the circuit

board and connected between a first pin on the memory repeater hub and the memory control unit. A second signal line is also formed on the selected layer of the circuit board and is connected to the first pin on the memory unit.

Other embodiments and advantages will become apparent from the description and claims that follow.

Description of the Drawings

FIG. 1 is a block diagram of a computer system.

FIG. 2 is a schematic diagram of a conventional signal routing scheme.

FIG. 3 is a schematic diagram of an improved signal routing scheme.

FIG. 4 is a cross-sectional view of a multi-layer circuit board having signal lines routed according to the scheme of FIG. 3.

Detailed Description

FIG. 3 shows a signal routing configuration that reduces the area required for each signal line 200 running between the MCU 120 and the memory unit. In this configuration, the signal line 200 has a width of approximately 18 mils with a 5 mil neck

down portion 205 contacting the corresponding pin 135 on the memory unit. The signal line 210 exiting the pin 135 also has a width of approximately 18 mils with a 5 mil neck down portion 215 contacting the pin 135. The two neck down portions 205, 215 run substantially parallel to each other for a distance, and then act an acute angle for another distance, the portions are separated by a gap 220. This gap 220 also has a width of approximately 5 mils. The neck down portions 205, 215 are not separated by a ground trace.

The gap 220 between the neck down portions 205, 215 provides the isolation between the signal lines 200, 210 yet reduces the area required to route the signal lines on a circuit board. Placing the gap 220, and not a ground trace, between the neck down portions 205, 215 can reduce congestion at the memory unit. This allows the signal lines 200, 210 into and out of the memory unit to be routed on a single layer of the circuit board on which the MCU and the memory unit reside. Routing the signal lines in this manner reduces the number of layers required to route signals between the MCU and the memory unit by a factor of two. As a result, the circuit board on which the MCU and memory unit reside can be less expensive to produce than conventional memory boards.

FIG. 4 shows the neck down portions 205, 215 of the signal line 200 on a multi-layer circuit board 225. The neck down portions 205, 215 into and out of the memory unit are formed on a single layer of the circuit board 225 and are separated by a gap 220 in which no traces are formed. No ground trace lies between the signal lines 205, 215. In some embodiments, ground traces 230, 235 lie on either side of the signal lines 205, 215 on the same layer of the circuit board 225. A ground plane 240 lies above or below the signal lines 205, 215 on another layer of the circuit board.

A number of embodiments have been described. Nevertheless, one of ordinary skill will understand that variations are possible. For example, while the invention has been described in terms of signal routing to a Rambus device, this scheme is useful in routing signals to other types of memory devices and even to other system components. Accordingly, other embodiments are within the scope of the following claims.

What is claimed is:

1. A computer system comprising:

a processor;

a memory unit configured to store data used by the processor;

a memory control unit configured to manage data flowing into and out of the memory unit;

a circuit board having multiple layers and comprising:

a first signal line, formed on a first layer of the circuit board and connected between a first connection on the memory unit and the memory control unit; and

a second signal line also formed on the first layer of the circuit board and connected to the first pin on the memory unit,

wherein said layer defines a non-grounded gap between said first and second lines

2. The system of claim 1, wherein at least a portion of the second signal line is routed roughly parallel to the first signal line.

3. The system of claim 1, further comprising third and fourth signal lines, on a second layer of the circuit board, different than the first layer.

4. The system of claim 2, wherein the first signal line and the portion of the second signal line that is routed roughly parallel to the first signal line have substantially equal widths.

5. The system of claim 4, wherein the first signal line and the portion of the second signal line that is routed roughly parallel to the first signal line are separated by a distance approximately equal to said widths.

6. The system of claim 5, wherein the widths of the lines and the distance separating the lines each approximately 5 mils.

7. The system of claim 1, wherein the memory unit

comprises a Rambus device.

8. A method for use in routing signals between a memory unit and a memory control unit, the method comprising:

delivering a first signal over a first signal line formed on a selected layer of a circuit board and connected between the memory control unit and on the memory unit;

delivering a second signal over a second signal line formed on the selected layer of the circuit board and connected to the first pin of the memory unit; and separating said first and second signal lines without a ground connection therebetween

9. The method of claim 8, wherein said delivering the second signal includes delivering the second signal over a portion of the second signal line that is routed roughly parallel to a portion of the first signal line.

10. The method of claim 8, further comprising delivering another signal to said memory control unit on another layer of

the circuit board over portions of the first and second signal lines that are not separated by any conductive traces.

11. The method of claim 8, wherein delivering the first signal and the second signal include delivering the signals over portions of the first and second signal lines that have substantially equal widths.

12. The method of claim 11, wherein delivering the first signal and the second signal include delivering the signals over portions of the first and second signal lines that are separated by a distance approximately equal to their widths.

13. The method of claim 12, wherein delivering the first signal and the second signal include delivering the signals over portions of the first and second signal lines that are approximately 5 mils wide and that are separated by a distance of approximately 5 mils.

14. A method for use in manufacturing a computer system, the method comprising:

forming a multiple-layer circuit board with first and second signal lines on a selected layer of the board;

connecting a memory unit to the board such that a first connection on the memory unit connects to the first and second signal lines; and

affixing a memory control unit to the board such that the memory control unit connects to at least the first signal line.

15. The method of claim 14, further comprising forming at least a portion of the second signal line to be roughly parallel to the first signal line.

16. The method of claim 14, further comprising forming the first and second conductive lines such that no conductive trace lies between the first signal line and the portion of the second signal line that is routed roughly parallel to the first signal line.

17. The method of claim 16, further comprising forming the first signal line and the portion of the second signal line that is routed roughly parallel to the first signal line to have substantially equal widths.

18. The method of claim 17, further comprising forming the first signal line and the portion of the second signal line that is routed roughly parallel to the first signal line to be separated by a distance approximately equal to their widths.

19. The method of claim 18, further comprising forming the signal lines such that the widths of the lines and the distance separating the lines are all equal to approximately 5 mils.

20. A circuit board for use in a computer system comprising:

a memory unit;

a memory control unit; and

a data bus connecting the memory control unit to the memory

unit and comprising:

a first signal line formed on a selected layer of the circuit board and connected to the memory control unit and to a first connection on the memory unit; and

a second signal line formed on the selected layer of the circuit board and also connected to the first connection on the memory control unit.

Abstract

A computer system includes a processor and a multi-layer circuit board having a memory unit, a memory control unit, and a data bus coupling the memory control unit to the memory unit. A first signal line is formed on a selected layer of the circuit board and connected between a first pin on the memory unit and the memory control unit. A second signal line is also formed on the selected layer of the circuit board and is connected to the first pin on the memory unit.

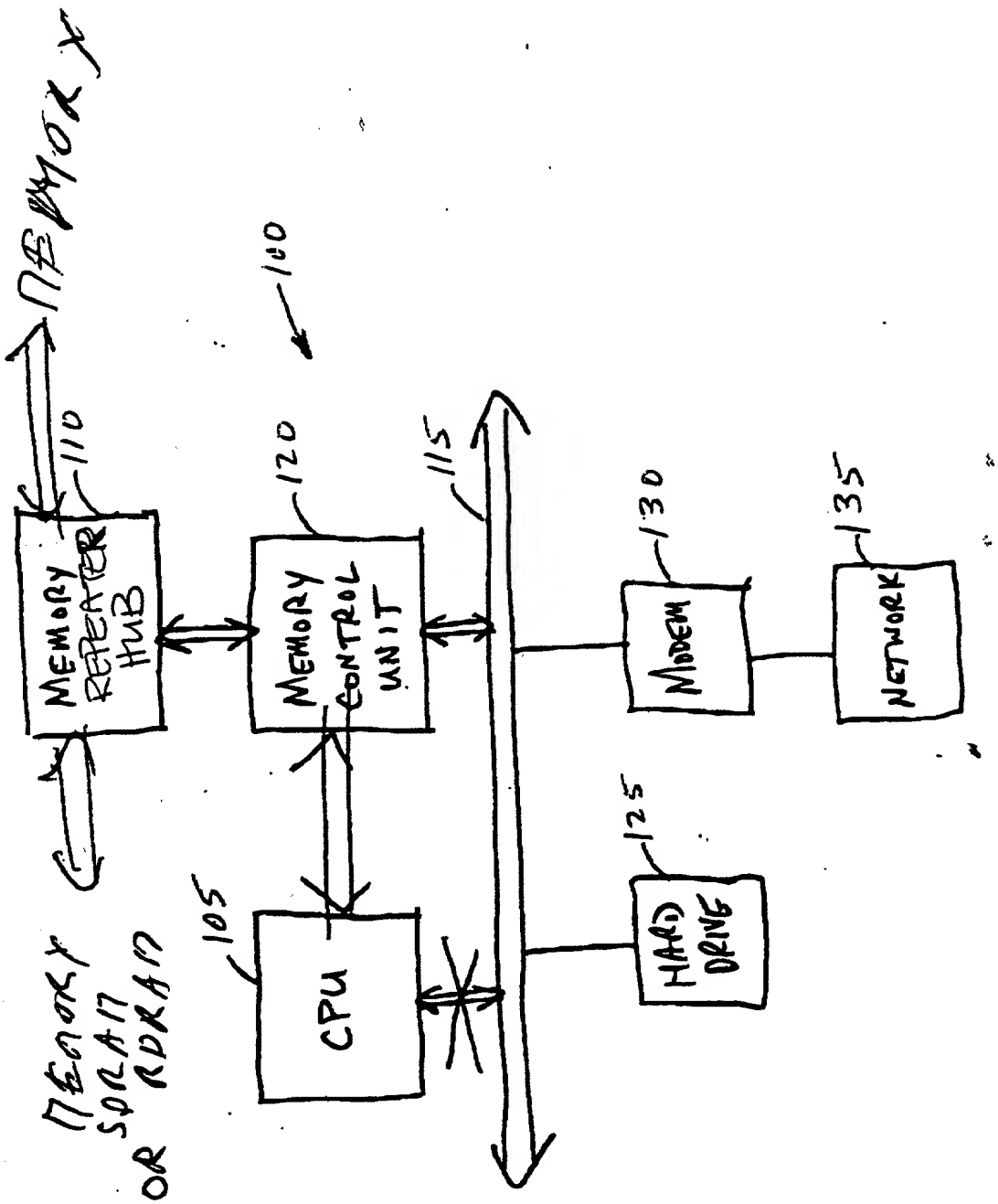
MEMORY
SDRAM
OR
RDRAM
105
CPU
MEMORY
REPEATER
HUB
110
MEMORY
CONTROL
UNIT
120
100
115
HARD
DRIVE
125
MODEM
130
NETWORK
135
TO NETWORK

FIG. 1

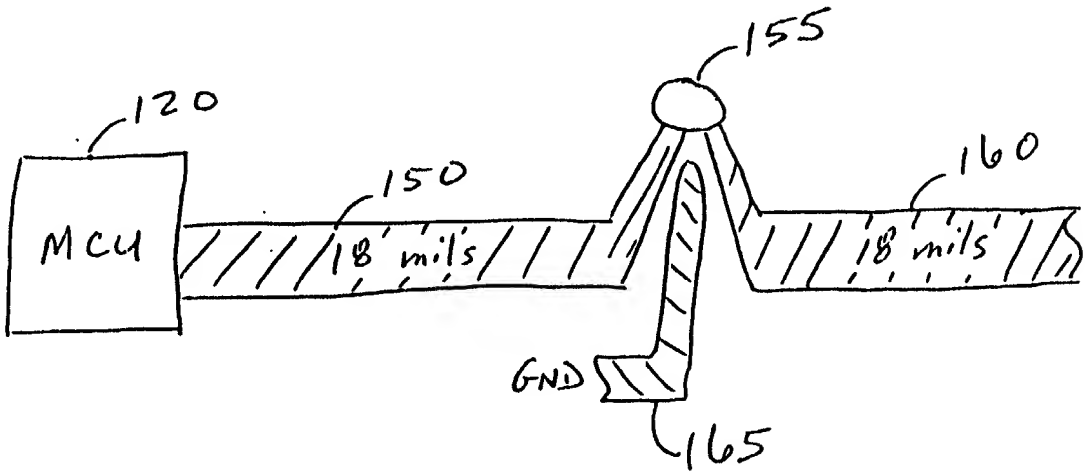

FIG. 2

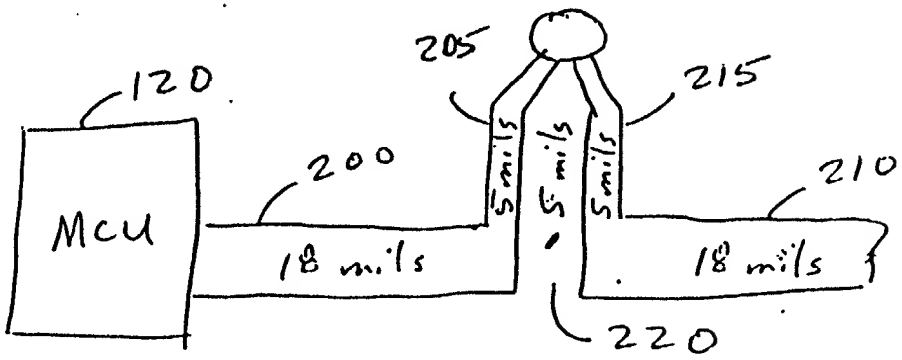

FIG. 3

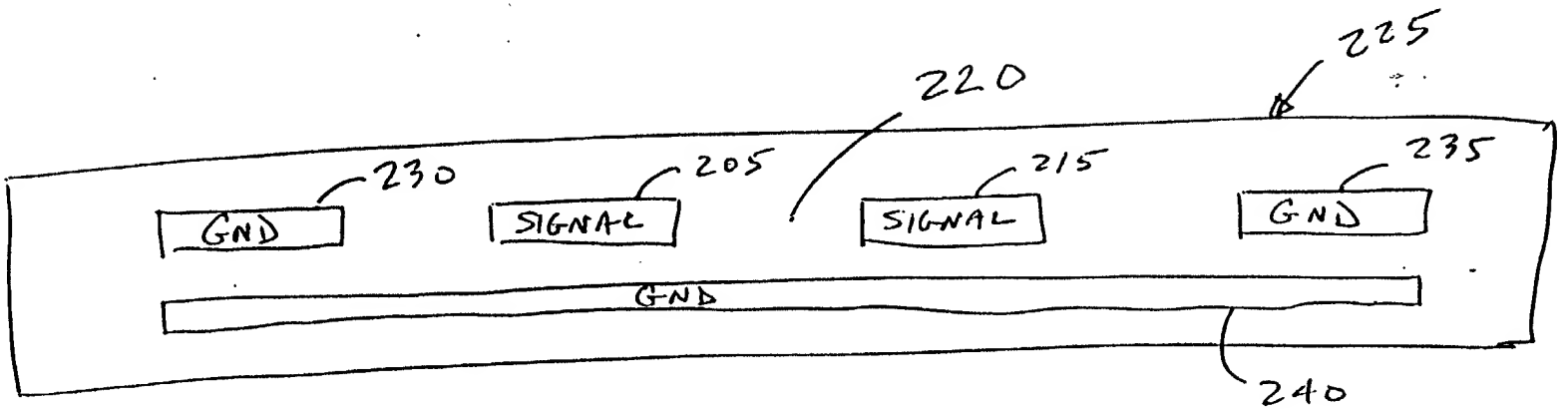

FIG. 4

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled IMPROVED SIGNAL ROUTING BETWEEN A MEMORY CONTROL UNIT AND A MEMORY DEVICE, the specification of which:

[X] is attached hereto.
[] was filed on _____ as Application Serial No. _____ and was amended on _____.
[] was described and claimed in PCT International Application No. _____ filed on _____ and as amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information I know to be material to patentability in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim the benefit under Title 35, United States Code, §119(e)(1) of any United States provisional application(s) listed below:

U.S. Serial No.	Filing Date	Status

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose all information I know to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

U.S. Serial No.	Filing Date	Status

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Country	Application No.	Filing Date	Priority Claimed
			[] Yes [] No
			[] Yes [] No

Combined Declaration and Power of Attorney

I hereby appoint the following attorneys and/or agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

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Inventor's Signature: Keith Dow Date: 12-10-99

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